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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/840,747	04/23/2001	Howard Sachs	021111000100	4810

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EXAMINER
BOWERS, BRANDON

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 09/11/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/840,747	Applicant(s) SACHS, HOWARD	
	Examiner Brandon W Bowers	Art Unit 2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 August 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) *1-10 and 27-32* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2,3* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of Group II – Claims 11-26 in Paper No. 5 is acknowledged. Cancellation of claims 1-10 and 27-32 is requested.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

Claims 11-13 are rejected under 35 U.S.C. 102(e) as being anticipated by Andreev et al., US Patent No. 6,182,272.

In reference to claim 11, Andreev teaches a method comprising obtaining cells, laying out cells and trace routing (Figure 3). Andreev describes cells as being a group of one or more circuit elements grouped to perform a function. The step of obtaining cells is equivalent to selecting an item, the item being a group or a function, for placement on a layout and selecting a further item for placement on a layout. The step of laying out cells is equivalent to placing the 1st and 2nd items on the layout. The step of trace routing is equivalent to defining interconnections between the 1st and 2nd items.

In reference to claims 12 and 13, Andreev teaches wherein the layout comprises a plurality of layers that are separated by metalization having vias (Figure 1, and Column 1, lines 42-49).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 14 to 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhen, US Patent No. 6,298,468 in view of Dangelo et al, US Patent No 5,880,971.

In reference to claim 14, Zhen teaches an integrated circuit comprised of a plurality of regularly placed circuit groups having predefined connection points with at least some of the groups being amalgamated into sets of groups (Figure 2). Zhen does not teach that the circuit groups are on the order of1000 gates. Dangelo teaches that design methodology wherein circuit groups are less than a few thousand gates (column 13, line 42). "on the order of a 1000 thousand gates" and a few thousand gates are deemed to be equivalent to one another. It would be obvious at the time of invention to incorporate the methodology of Dangelo wherein circuit groups are less than a few thousand gates with the integrated circuit of Zhen comprised of a plurality of regularly placed circuit groups having predefined connection points with at least some of the groups being amalgamated into sets of groups to make an integrated circuit comprised of a plurality of regularly placed circuit groups, the circuit groups being on an order of

magnitude of 1000 gates, the circuit groups having predefined connection points with at least some of the groups being amalgamated into sets of groups because the seemingly insurmountable job of designing a highly complex circuit is broken into small, workable design projects on an order on magnitude of 1000 gates.

In reference to claims 15-18, Zhen teaches that glue logic is used to connect the groups together (column 5, lines 35-36). Glue logic refers to the electronic circuitry required to interface two or more circuit blocks. When circuit blocks are assembled into a larger circuit, it is common to put electronic circuitry (or electrical connections) between the circuit blocks to couple and make them operate together. The circuitry that sits between circuit blocks is called glue logic. Glue logic is equivalent to trailers and provides physical translation, buffering, and staging of interface signals associated with the predefined connection points of circuit blocks.

Claims 19-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhen, US Patent No. 6,298,468 in view of Dangelo et al, US Patent No 5,880,971 as applied to claim 14 above, and further in view of Block et al., Us Patent No 6,397,375.

In reference to claim 19, Zhen in view of Dangelo does not teach wherein the integrated circuit has a number of metal layers, with a plurality of circuit groups on a first plurality of metal layers and clock and power signals on metal layers other than the first plurality of metal layers. Block teaches a plurality of metal layers wherein circuit groups and intra-block routing is on the lowest levels, while inter-block routing is on the higher level. Additionally clock and power signals are on all layers (Column 2, lines 4-11).

Accordingly, Block teaches wherein the integrated circuit has a number of metal layers, with a plurality of circuit groups on a first plurality of metal layers and clock and power signals on metal layers other than the first plurality of metal layers. Accordingly it would be obvious at the time of invention to integrate the circuit as taught by Block wherein the integrated circuit has a number of metal layers, with a plurality of circuit groups on a first plurality of metal layers and clock and power signals on metal layers other than the first plurality of metal layers with the integrated circuit of Zhen and Dangelo as described above in claim 14 to create an integrated circuit comprised of a plurality of regularly placed circuit groups, the circuit groups being on an order of magnitude of 1000 gates, the circuit groups having predefined connection points with at least some of the groups being amalgamated into sets of groups wherein the integrated circuit has a number of metal layers, with a plurality of circuit groups on a first plurality of metal layers and clock and power signals on metal layers other than the first plurality of metal layers because as integrated circuits of increasingly higher densities have been developed, more metal layers and interconnects per layer are required.

In reference to claims 20-22, Block teaches wherein clock and power signals are on the same layer, wherein global routing signals are on a different layer than the first plurality of layers and the clock and power signals, and the global routing signals are on a plurality of layers (Column 2, lines 4-11).

In reference to claims 23-26, Dangelo teaches wherein the groups comprise data path groups, memory groups, control groups, I/O groups, and analog groups (Figure 1 and column 7, lines 7-54).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brandon W Bowers whose telephone number is (703)305-4387. The examiner can normally be reached on 8:30 am until 5:00 pm Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (703)308-1323. The fax phone numbers for the organization where this application or proceeding is assigned are (703)872-9318 for regular communications and (703)872-9313 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-1782.

BWB
August 29, 2002

VUTHE SIEK
PRIMARY EXAMINER